Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT8002-3 (MLPAK33) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- Fully automotive qualified to AEC-Q101 at 175°C
- Side-wettable flanks for optical solder inspection

3. Applications

- LED Lighting
- Switching circuits
- DC-DC conversion

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	60	V
V_{GS}	gate-source voltage	DC; T _j ≤ 175 °C		-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	[1]	-	-	21	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	-	27	W
Static charact	eristics						·
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5.6 \text{ A}; T_j = 25 \text{ °C}$		-	23.7	29	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{DS} = 30 \text{ V}; I_D = 5.6 \text{ A}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ °C}$		-	2.4	-	nC

^{[1] 21} A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	1 2 3 4	
2	S	source	<u> </u>	
3	S	source		D ⊥
4	G	gate		
5	D	drain		
6	D	drain		mbb076 S
7	D	drain	8 7 6 5	
8	D	drain	MLPAK33 (SOT8002-3)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BUK9Q29-60E		plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3			

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Q29-60E	7AA

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	60	V
V_{GS}	gate-source voltage	DC; T _j ≤ 175 °C		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	[1]	-	21	А
		V _{GS} = 10 V; T _{mb} = 100 °C		-	14.5	А
I _{DM}	peak drain current	single pulse; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	84	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	27	W
T _j	junction temperature			-55	175	°C
T _{stg}	storage temperature			-55	175	°C
Source-drain	diode					
Is	source current	T _{mb} = 25 °C	[1]	-	21	А
I _{SM}	peak source current	single pulse; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$	[1]	-	84	Α

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
E _{DS(AL)S}		V_{sup} < 60 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω ; I_{D} = 15.8 A; unclamped	[2] [3]	-	25	mJ

- [1] 21 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.

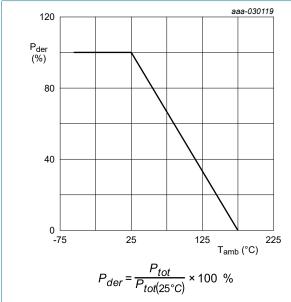


Fig. 1. Normalized total power dissipation as a function of ambient temperature

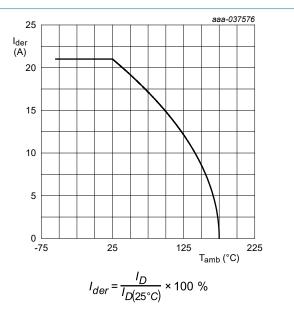


Fig. 2. Continuous drain current as a function of ambient temperature

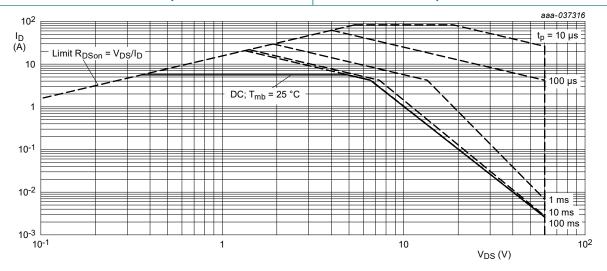
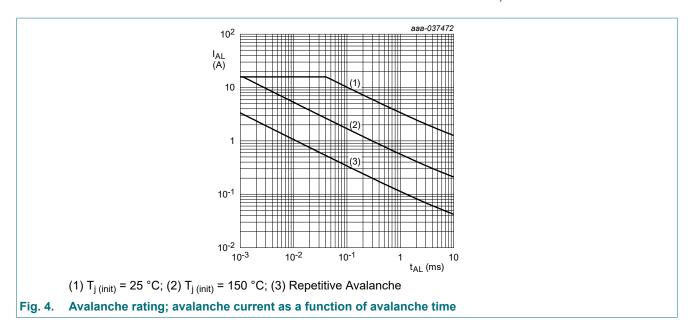


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

60 V, N-channel Trench MOSFET



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
uig-iiib)	thermal resistance from junction to mounting base		-	3.5	5.5	K/W	

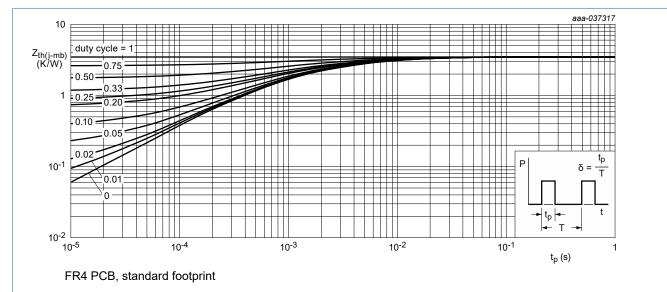


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1.3	1.7	2.1	V
I _{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-	1	μΑ
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 125 °C	-	-	20	μΑ
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	400	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	0.1	μΑ
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-0.1	μΑ
R _{DSon}	drain-source on-state	V_{GS} = 10 V; I_D = 5.6 A; T_j = 25 °C	-	23.7	29	mΩ
	resistance	V _{GS} = 10 V; I _D = 5.6 A; T _j = 105 °C	-	39	51.4	mΩ
		V _{GS} = 10 V; I _D = 5.6 A; T _j = 125 °C	-	42.4	55.9	mΩ
		V _{GS} = 10 V; I _D = 5.6 A; T _j = 175 °C	-	52	64	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 4.9 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	28	38	mΩ
		V _{GS} = 4.5 V; I _D = 4.9 A; T _j = 105 °C	-	45.3	63.9	mΩ
		V _{GS} = 4.5 V; I _D = 4.9 A; T _j = 125 °C	-	49.2	69.5	mΩ
		V _{GS} = 4.5 V; I _D = 4.9 A; T _j = 175 °C	-	60.9	83.6	mΩ
9 _{fs}	forward transconductance	$V_{DS} = 5 \text{ V}; I_D = 5.6 \text{ A}$	-	18.6	-	S
R_G	gate resistance	f = 1 MHz	-	2	-	Ω
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	V _{DS} = 30 V; I _D = 5.6 A; V _{GS} = 10 V;	-	12	18	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	1.6	-	nC
Q_{GD}	gate-drain charge		-	2.4	-	nC
C _{iss}	input capacitance	V _{DS} = 30 V; f = 1 MHz; V _{GS} = 0 V;	-	660	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	67	-	pF
C _{rss}	reverse transfer capacitance	_	-	40	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; I _D = 5.6 A; V _{GS} = 10 V;	-	3	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	4	-	ns
t _{d(off)}	turn-off delay time	1	-	13	-	ns
t _f	fall time	1	-	5	-	ns
Source-dra	in diode	•			<u> </u>	
V _{SD}	source-drain voltage	I _S = 2.5 A; V _{GS} = 0 V; T _j = 25 °C	-	0.8	1	V
t _{rr}	reverse recovery time	$I_S = 2.5 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	13	-	ns
Q _r	recovered charge	V_{GS} = 10 V; V_{DS} = 30 V; T_j = 25 °C	_	7	_	nC

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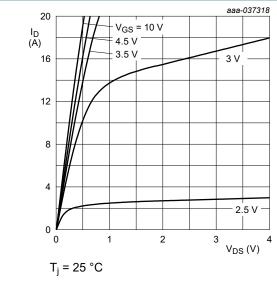


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

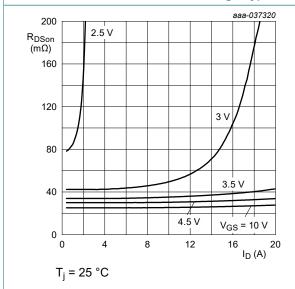


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

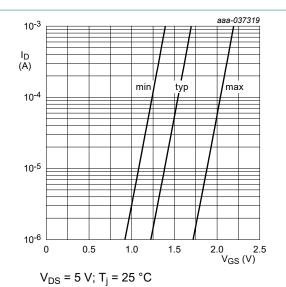


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

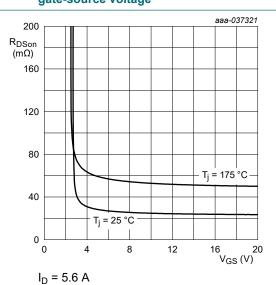


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

60 V, N-channel Trench MOSFET

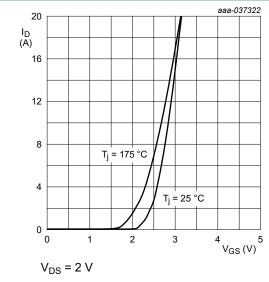


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

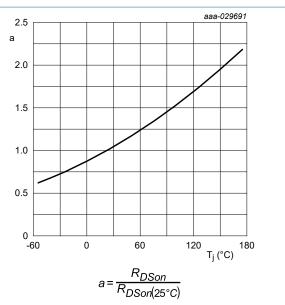


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

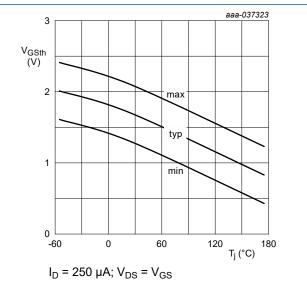
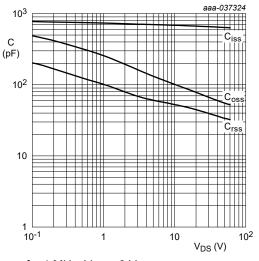


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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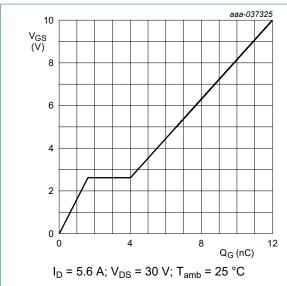


Fig. 14. Gate-source voltage as a function of gate charge; typical values

 $V_{GS} = 0 V$

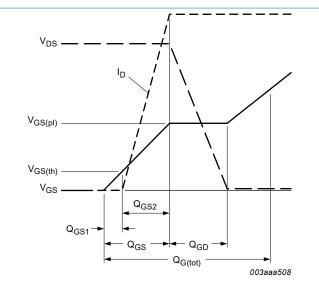


Fig. 15. Gate charge waveform definitions

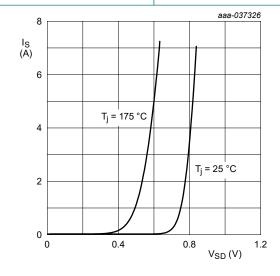
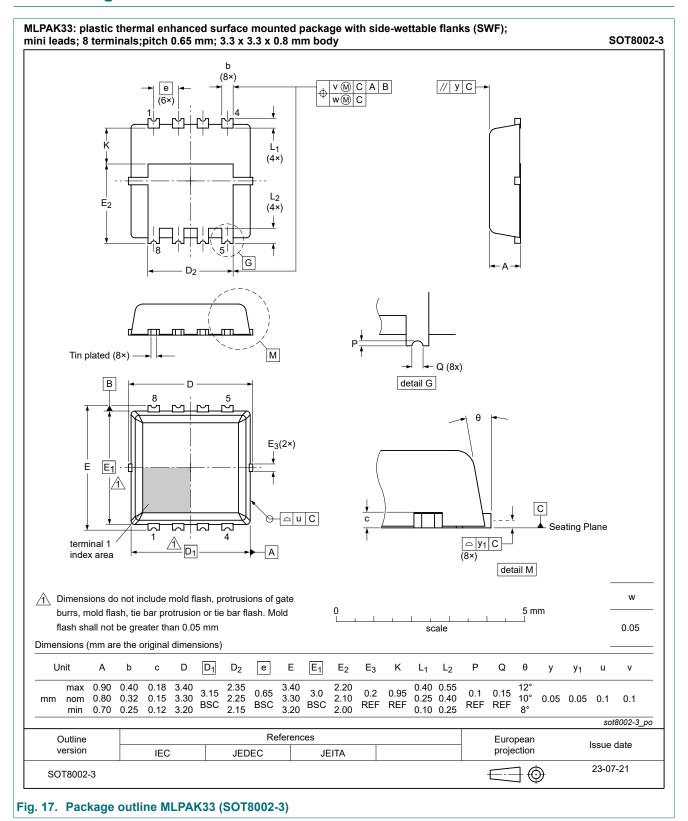


Fig. 16. Source current as a function of source-drain voltage; typical values

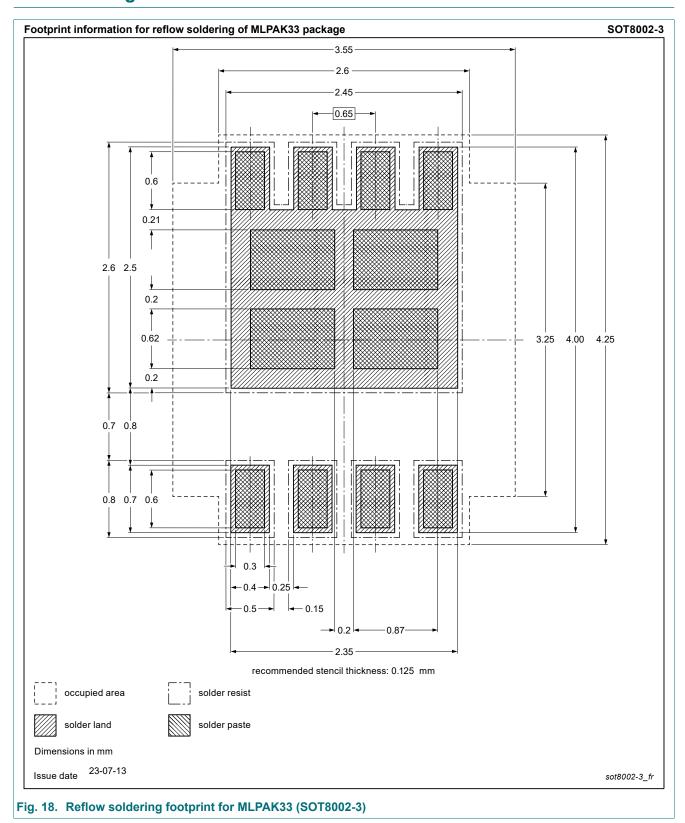
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11. Package outline



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12. Soldering



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13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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